In re Patent Application of:
ARNAUD ET AL.
Serial No. **09/886,966**
Filing Date: **JUNE 21, 2001**

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. Claim 8 has been amended to correct a typographical error. The arguments supporting patentability of the claims are presented in detail below.

I. Independent Claims 4, 7 And 23 Are Patentable

The Examiner rejected independent Claims 4 and 7 over the Wendelrup et al. patent in view of the Gardner et al. patent. The Examiner also rejected independent Claim 23 over the Wendelrup et al. patent alone. Since independent Claim 23 also recites first and second fractional-division phase-locked loops (as in Claims 4 and 7), this claim is being addressed herein.

The present invention, as recited in independent Claim 4, for example, is directed to a process for reducing electrical consumption of a transmitter/receiver device comprising a frequency synthesizer stage controlled by an automatic frequency control algorithm. The process comprises generating at least one reference signal for a transmission/reception stage within the transmitter/receiver device. The at least one reference signal has a first accuracy and is generated based upon at least one first fractional-division phase-locked loop within the frequency synthesizer stage.

The process further comprises generating a clock signal based upon a second fractional-division phase-locked loop within the frequency synthesizer stage, and generating a base signal for the at least one first fractional-division phase-locked loop and the second fractional-division phase-

locked loop. The base signal has a second accuracy less than the first accuracy. The base signal is delivered as a master-clock signal to a modulator/demodulator connected to the transmission/ reception stage when the transmission/reception stage and the second fractional-division phase-locked loop are inactive. The clock signal is delivered as the master-clock signal when the transmission/reception stage and the second fractional-division phase-locked loop are active.

Independent Claim 7 is similar to independent Claim 4 except the first and second fractional-division phase-locked loops (in Claim 4) have been replaced with first and second circuits. Independent Claim 23 is a device claim similar to independent method Claim 4.

Referring now to the Wendelrup et al. patent, the Examiner cited the background section (column 1) as disclosing a frequency synthesizer stage controlled by an automatic frequency control algorithm. The Examiner further states that Wendelrup et al. discloses the generation of a reference signal for a transmission/reception stage, wherein the reference signal is generated based upon a first fractional-division phase-locked loop. In addition, the Examiner states that a clock signal is generated based upon a second fractional-division phase-locked loop.

As correctly noted by the Examiner, Wendelrup et al. fails to disclose the generation of a base signal for the first and second fractional-division phase-locked loops. Wendelrup et al. also fails to disclose delivery of the base signal as a master-clock signal to a modulator/demodulator connected to the transmission/reception stage when the transmission/reception stage and the second fractional-

division phase-locked loop are inactive, and delivering the clock signal as the master-clock signal when the transmission/reception stage and the second fractional-division phase-locked loop are active. The Examiner cited the Gardner et al. patent as disclosing these features.

In FIG. 5 of the Gardner et al. patent, the reference clock **150** is set at 13 MHz, and there is also a 32 kHz clock **151**. Both clocks are input into the sleep logic **152**. When the mobile station is not in a sleep mode, the 13 MHz clock serves as a reference directly for the DSP registers **155**, the control process registers **157**, the TDMA timer **158**, and the sleep logic **152**. A first phase lock loop **162** up-converts the 13 MHz signal as a reference for the DSP **163**, while a second phase lock loop **164** up-converts the 13 MHz signal as a reference for the control processor **165**. The 13 MHz signal also acts as a reference for the mixed signal **166**. During the sleep mode, the 13 MHz clock is shut down, leaving only a free running 32 kHz clock.

The Applicants respectfully submit that even if the references were combined as suggested by the Examiner, the claimed invention is still not produced. First, the Examiner states that Wendelrup et al. discloses in column 1 first and second fractional-divisional phase-locked loops. In column 1, line 48 of Wendelrup et al., there is reference to only one phase-locked loop.

In the Gardner et al. patent, the Examiner has taken the position that two fractional-divisional phase-locked loops are disclosed in column 8, lines 14-24. However, reference is only made to one phase-locked loop in column 8, lines 19-20. Nonetheless, two phase-locked loops are shown in FIG. 5 of

Gardner et al. patent, but these two phase-locked loops are controlled by the same 13 MHz clock signal **150**. It will be assumed that the base signal being generated for the first and second fractional-divisional phase-locked loops **162, 164** is the 13 MHz signal being applied to both of these phase-locked loops.

The Examiner further states that in Gardner et al., the base signal is delivered as a master-clock signal to a modulator/demodulator connected to the transmission/reception stage when the transmission/reception stage and the second fractional-divisional phase-locked loop are inactive, and delivers the clock signal as the master clock signal when the transmission/reception stage and the second fractional-divisional phase-locked loop are active.

The Applicants respectfully submit that the Examiner has mischaracterized the Gardner et al. patent. Reference is directed to column 5, lines 26-28 of Gardner et al., which provides:

> "During sleep mode, the digital-to-analog converter and the 13 MHz oscillator are powered down, leaving only a free running 32 kHz clock." (Emphasis added.)

If the second fractional-divisional phase-locked loop (**162** or **164**) is inactive, then the oscillator providing the 13 MHz clock signal is also inactive - consequently, the base signal cannot be delivered as in the claimed invention.

Accordingly, it is submitted that independent Claim 4 is patentable over the Wendelrup et al. patent in view of the Gardner et al. patent. Independent Claim 7 is similar to

independent Claim 4, and it is submitted that this claim is also patentable over the Wendelrup et al. patent in view of the Gardner et al. patent. Independent Claim 16 is similar to independent Claim 4, and it is submitted that this claim is patentable over the Wendelrup et al. patent.

II. Independent Claims 16 And 26 Are Patentable

The Examiner rejected independent Claims 16 and 26 over the Wendelrup et al. patent. The present invention, as recited in independent Claim 16, for example, is directed to a process for reducing electrical consumption within a transmitter/receiver device. The process comprises generating at least one first clock signal at a first accuracy at a first power level for a transmission/reception stage and a modulator/demodulator when the transmission/reception stage is active, and generating a second clock signal at a second accuracy less than the first accuracy and at a second power level less than the first power level for the modulator/demodulator when the transmission/reception stage is inactive.

Independent Claim 26 is a device claim similar to independent method claim 16.

Referring now to the Wendelrup et al. patent, the Examiner cited the background section (column 1) and FIG. 4 as disclosing a method for reducing electrical consumption within a transmitter/receiver device. The Examiner further states that Wendelrup et al. discloses generating at least one first clock signal **12** for a transmission/reception stage and a modulator/demodulator when the transmission/reception stage is active, and generating a second clock signal **10** for the modulator/demodulator when the transmission/reception stage is

inactive.

As illustrated in FIG. 4 of the Wendelrup et al. patent, a phase detector **22** provides a digital output to a charge pump **24**. The output of the charge pump **24** is filtered in a low-pass filter **26** and fed back to RTC **10** to control the frequency of the lower power clock. It appears that the Examiner has assumed that the transmission/reception stage is active when the first clock signal **12** is generated, and the transmission/reception stage is inactive when the second clock signal **10** is generated.

The Applicants respectfully submit that Wendelrup et al. fails to mention when the transmission/ reception stage is active or inactive. Wendelrup et al. discloses that during a standby or idle mode, the high frequency master clock **12** is powered down, and system timing is maintained by the lower frequency clock **10**. However, no reference is made as to when the transmission/reception stage would be active or inactive. Wendelrup et al. emphasizes that system timing is maintained in the lower power mode.

In contrast, independent Claim 16 recites that the first clock signal is generated when the transmission/ reception stage is active, and that the second clock signal is generated when the transmission/reception stage is inactive.

Accordingly, it is submitted that independent Claim 16 is patentable over the Wendelrup et al. patent. Independent Claim 26 is similar to independent Claim 16, and it is submitted that this claim is also patentable over the Wendelrup et al. patent. In view of the patentability of the independent claims as discussed above, it is submitted that their dependent claims, which recite yet further

distinguishing features, are also patentable over the prior art. Thus, these dependent claims require no further discussion herein.

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CONCLUSION

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents on this 22 day of July, 2004.

Michael W. Taylor